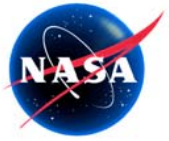


Cross Functional Design Tools for Radiation Mitigation and Power Optimization of FPGA Circuits

Matthew French[1], Paul Graham[3], Michael Wirthlin[2], and Li Wang[1]

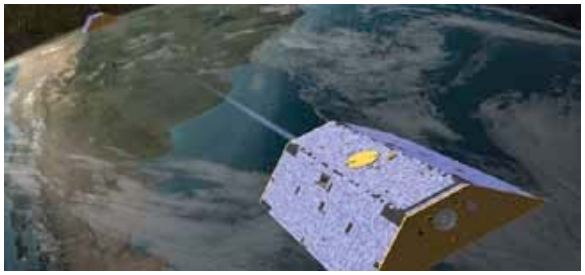
University of Southern California, Information Sciences Institute[1]

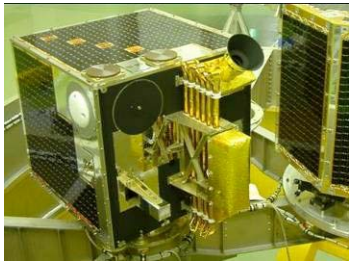
Brigham Young University[2]

Los Alamos National Laboratory[3]

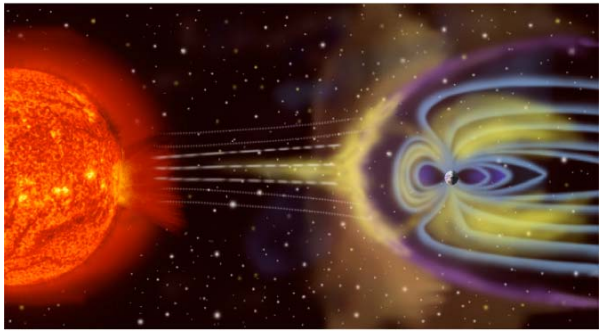
COTS SRAM-Based FPGAs in Space

- **Advantages**
  - 10-100x Processing Performance over Anti-fuse FPGAs
  - Reprogrammable
    - Resource Multiplexing
      - Multi-mission, multi-sensor
    - Mission Obsolescence
      - Update Algorithms
    - Design Flaws
      - Correct in Orbit
- **Gaining Popularity in Space Systems**
  - MARS 2003 Lander (JPL); XQR4062XL
  - MARS 2003 Rover (JPL); XQVR1000
  - GRACE (GSFC); XQR4036XL
  - FedSat (Univ. of Australia); XQR4036XL
  - OPTUS (Raytheon); XQVR300





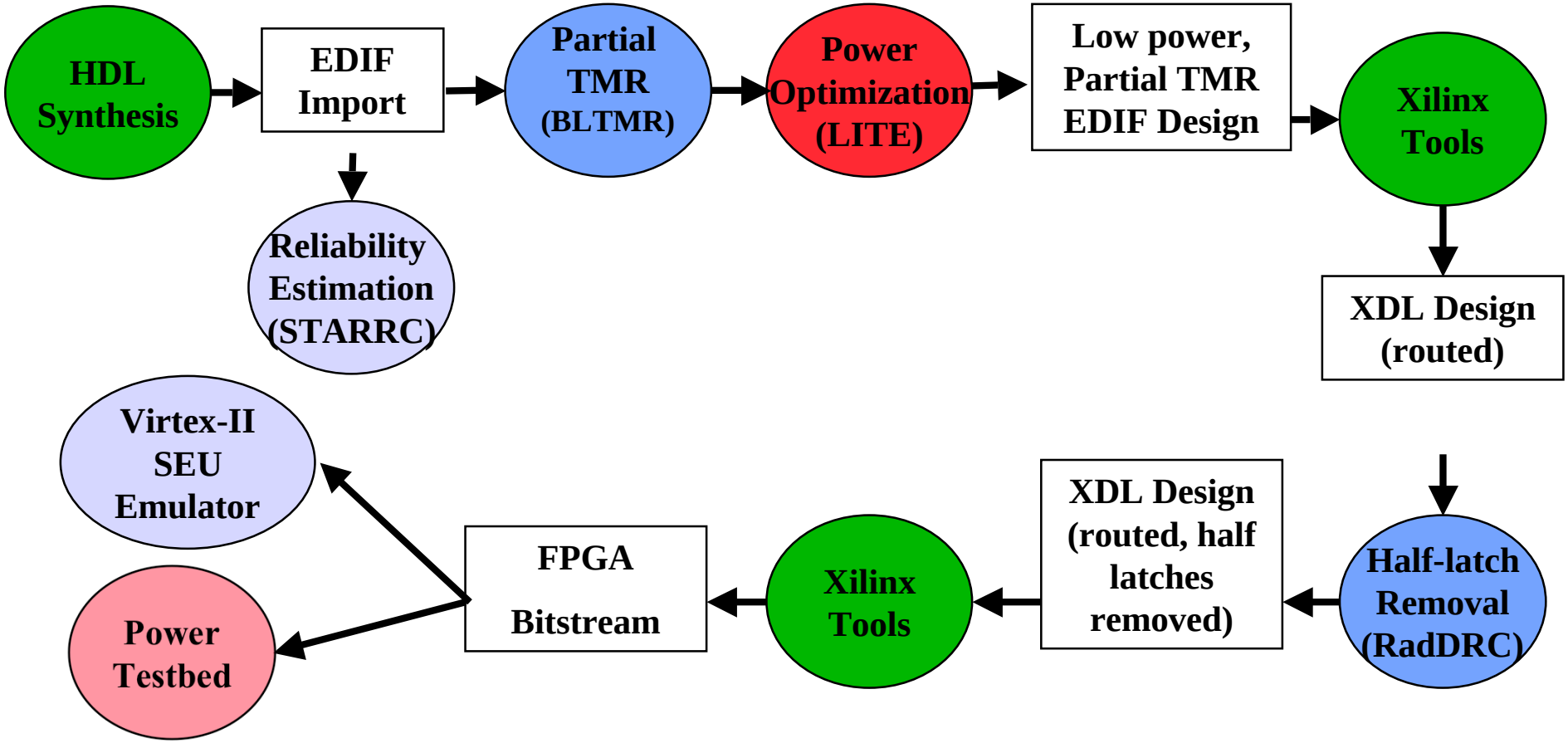
Disadvantages of SRAM-Based FPGAs in Space



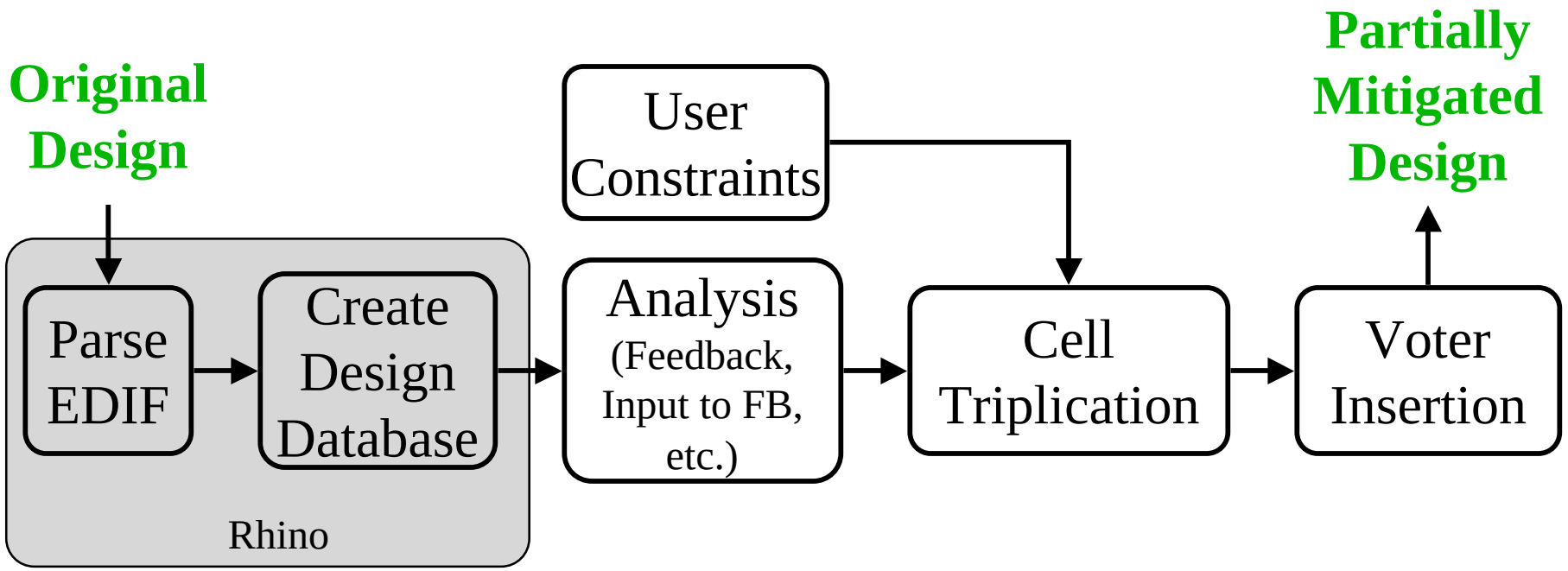
- **Radiation Effects**
  - Configuration and Logic are susceptible
  - Single Event Upset (SEU)
  - Single Event Functional Interrupt (SEFI)
- **Power**
  - Antifuse is more power savvy (20-50% less)
  - Greater Horsepower = Greater Power Consumed
- **SRAM FPGAs vs Anti-fuse FPGAs**
  - Benefits
    - ~10x-100x Performance Gain
    - ~10x Cost Savings
    - ~100-1000x Price Performance Gain
  - Costs
    - Need Software Tools

Can we develop software tools to BOTH mitigate radiation effects AND lower power consumption?

Radiation Design and Verification Flow

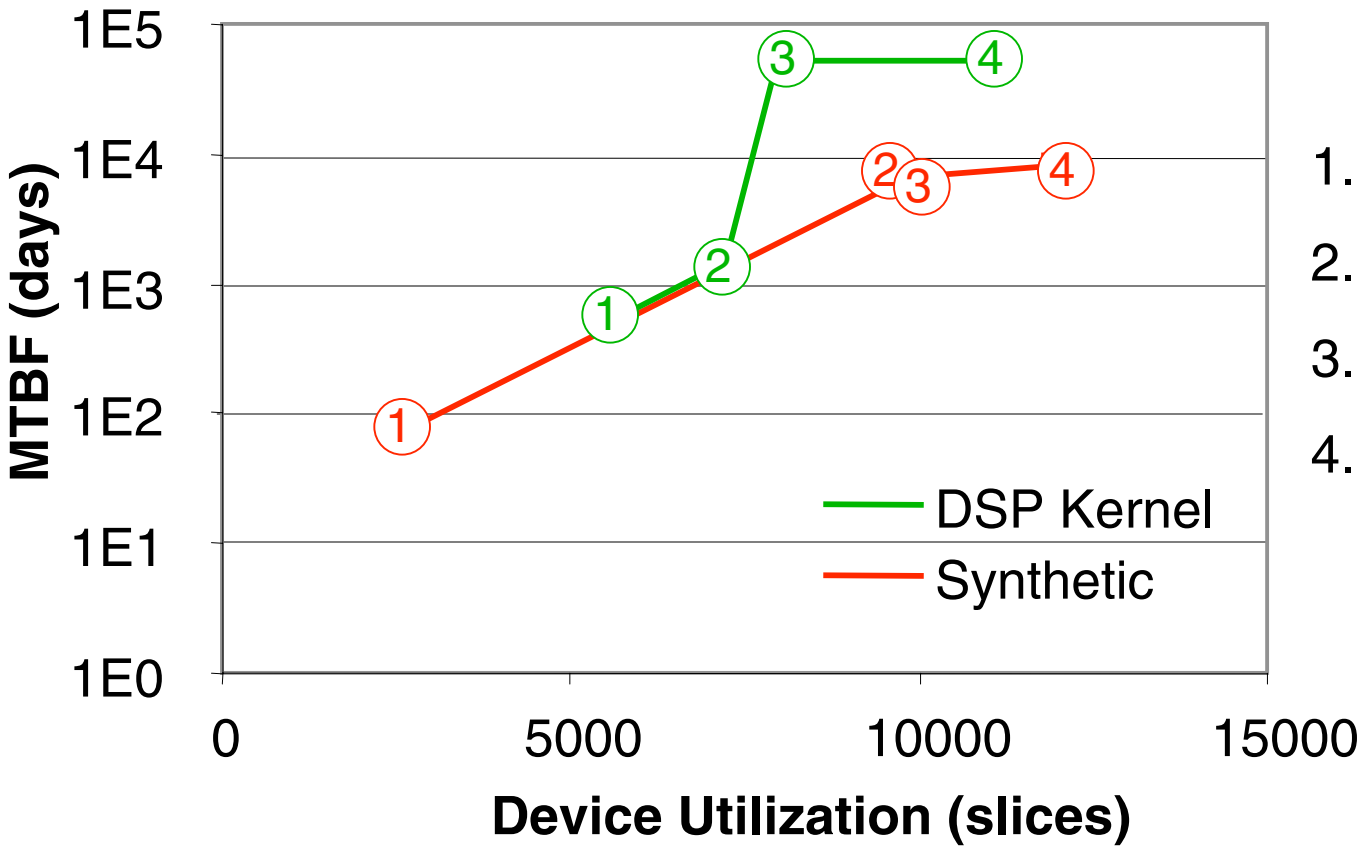


BYU LANL TMR Tool (BLTMR)



- **Typically 3 levels of mitigation**
  - **Feedback paths**
  - **Input and Feedback paths**
  - **Full TMR**
- **Focused on persistent error mitigation**

Experimental Results – MTBF vs. Mitigation Level



Mitigation Level

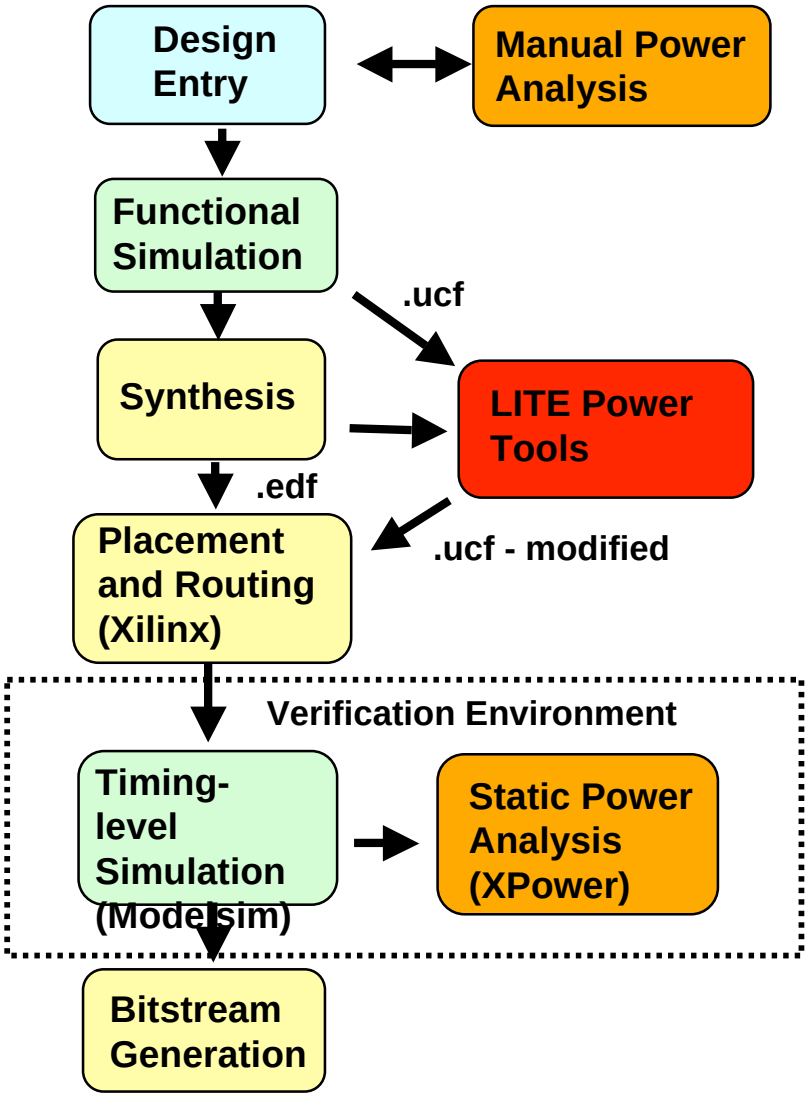
1. Unmitigated
2. Feedback TMR
3. Feedback+Input TMR
4. Max TMR

- AP-8 Solar Minimum, JPL Solar Proton Quiet, CRÈME 96 Solar Minimum
- GPS orbit (22,200 km altitude, 55° inclination)

Brian Pratt, Michael Caffrey, Paul Graham, Keith Morgan, and Michael J. Wirthlin, *"Improving FPGA Design Robustness with Partial TMR"*, IEEE International Reliability Physics Symposium (IRPS) pp. 226-232, April 2006.

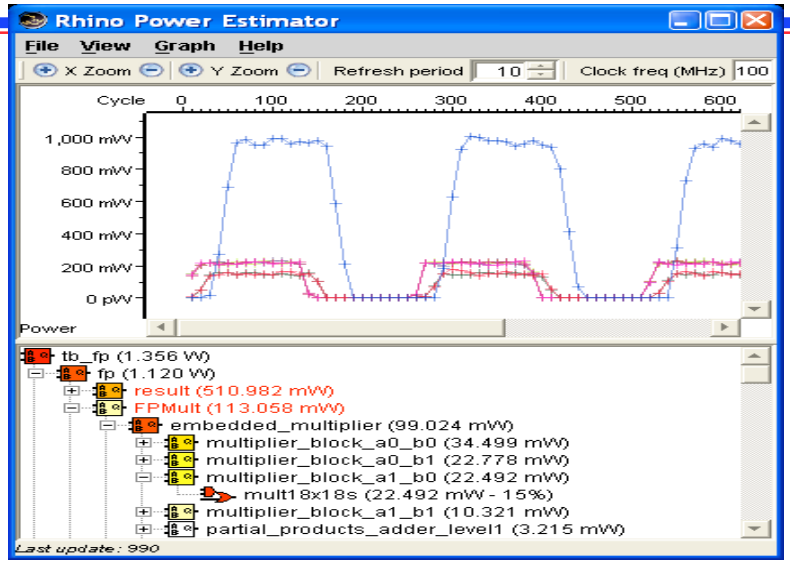
Power Optimization Approach

- **Approach:**
  - Interoperate with existing tool flows
  - No circuit functionality modifications
  - Single pass optimizations
- **Provide power data to Placement and Routing tools**
- **Translate power to timing or placement constraints**
  - Minimize clock/wire lengths of high power nets
- **Developed 4 optimization algorithms**
  - Clock tree paring, Slack minimization, 2-terminal net co-location, Area minimization
- **Verify power optimization approaches**



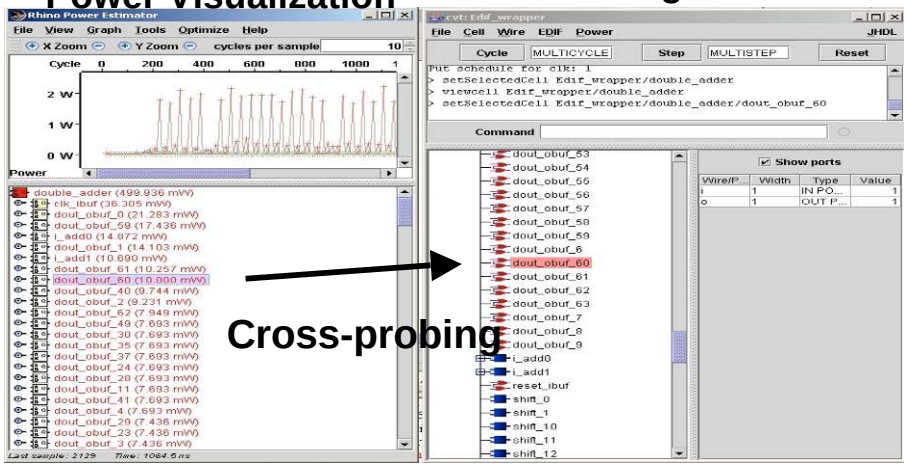
Low-power Intelligent Tool Environment (LITE)

- CAD tool for power investigation and optimization
- Two views:
  - Instantaneous vs. cumulative power consumption over time
  - Sorted tree view of worst offenders
- More rapidly identify inefficient circuits and operating modes
- Simulation trigger on power specification
- Integrated cross-probing with existing JHDL tools
  - Unified Environment
  - Allows Rapid Experimentation
  - Smart Re-use of CPU Memory



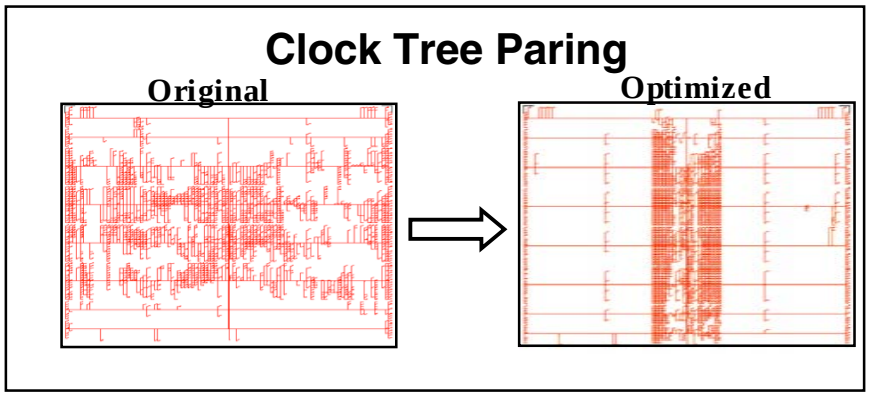
Power Visualization

JHDL Design Environment



Low-power Intelligent Tool Environment (LITE) Power Optimization Results

- Techniques do not modify functionality
- Compliant with COTS tool flow
- Original user constraints maintained
- Techniques can be combined



M. French, L. Wang, M. Wirthlin, "Power Visualization, Analysis, and Optimization Tools for FPGAs," IEEE Symposium on Field-Programmable Custom Computing Machines, April 2006.

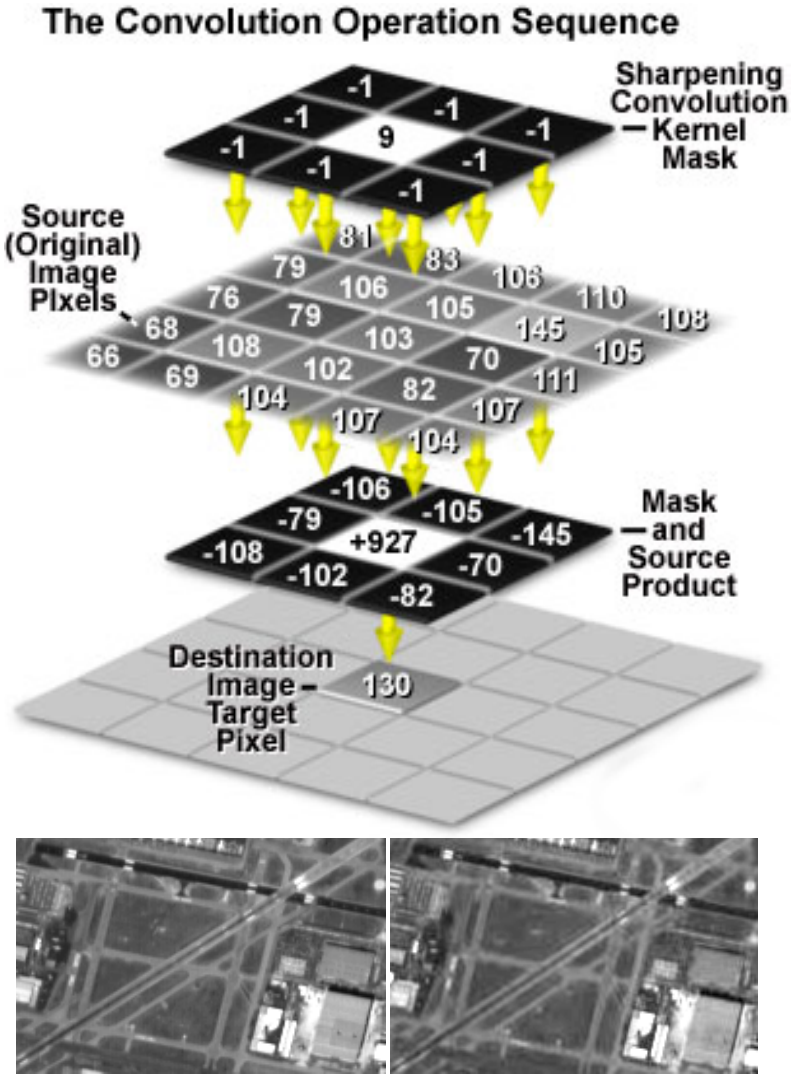
Benchmark Suite Results

Design	Baseline Power (mW)	Max Power Reduction	Max Power Saved (mW)
crc	31.3	6.7%	2.1
fm	102	2.9%	2.9
vga	138	12.7%	17
usbf	81.7	10.7%	8.8
pci	38.8	19.4%	7.6
rhino	163	7.1%	8.5
des3	139	8.6%	12
l1	643	3.3%	21
S1	251	10.7%	27
S2	1020	19.4%	198

Up to 19.4% maximum power reduction.
Average power reduction is 10.2%.

Benchmark Application

- 3x3 Image Convolution
  - 1024 x 1024, 8 bit
  - Metrics: throughput, power, reliability
- Consider both kernel and system implementation
  - Memory, I/O accesses
  - State Machines
  - System Throughput, Power …



Partial TMR Resource Utilization

Design Name	Slice Usage (%)	FF		LUT		MULT/BRAM	
		Count	Size Growth	Count	Size Growth	Count	Size Growth
Baseline	16	1178	1	685	1	9/3	1
Partial BLTMR	39	1749	x1.5	2123	x3.1	9/3	x1
Full BLTMR	77	3535	x3.0	2653	x3.9	27/9	x3

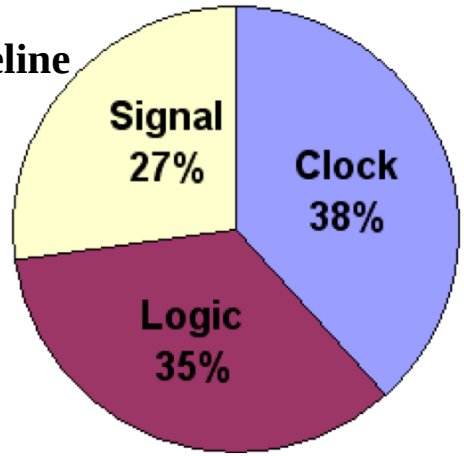
Target Device: Virtex-II 1000

- **Partial-BLTMR TRAD:**
  - 35% cells are triplicated, 1870 new instances are added
- **Full-BLTMR TRAD:**
  - 100% cells are triplicated, 5342 new instances are added

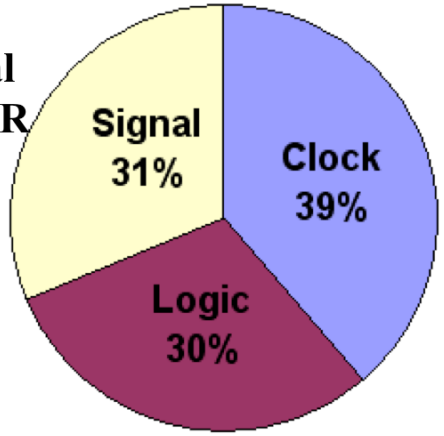
Benchmark Power Distribution

Design Name	Total		Clock		Logic		Signal	
	mW	Power Growth	mW	Power Growth	mW	Power Growth	mW	Power Growth
Baseline	22.5	1	8.5	1	7.7	1	6.0	1
Partial BLTMR	33.9	x1.5	13.1	x1.5	10.0	x1.3	10.6	x1.8
Full BLTMR	81.6	x3.6	32.0	x3.8	25.3	x3.3	24.0	x4.0

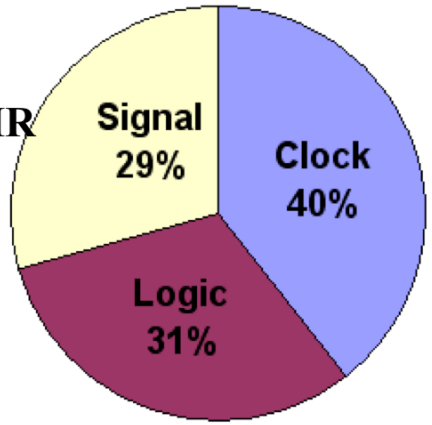
Baseline



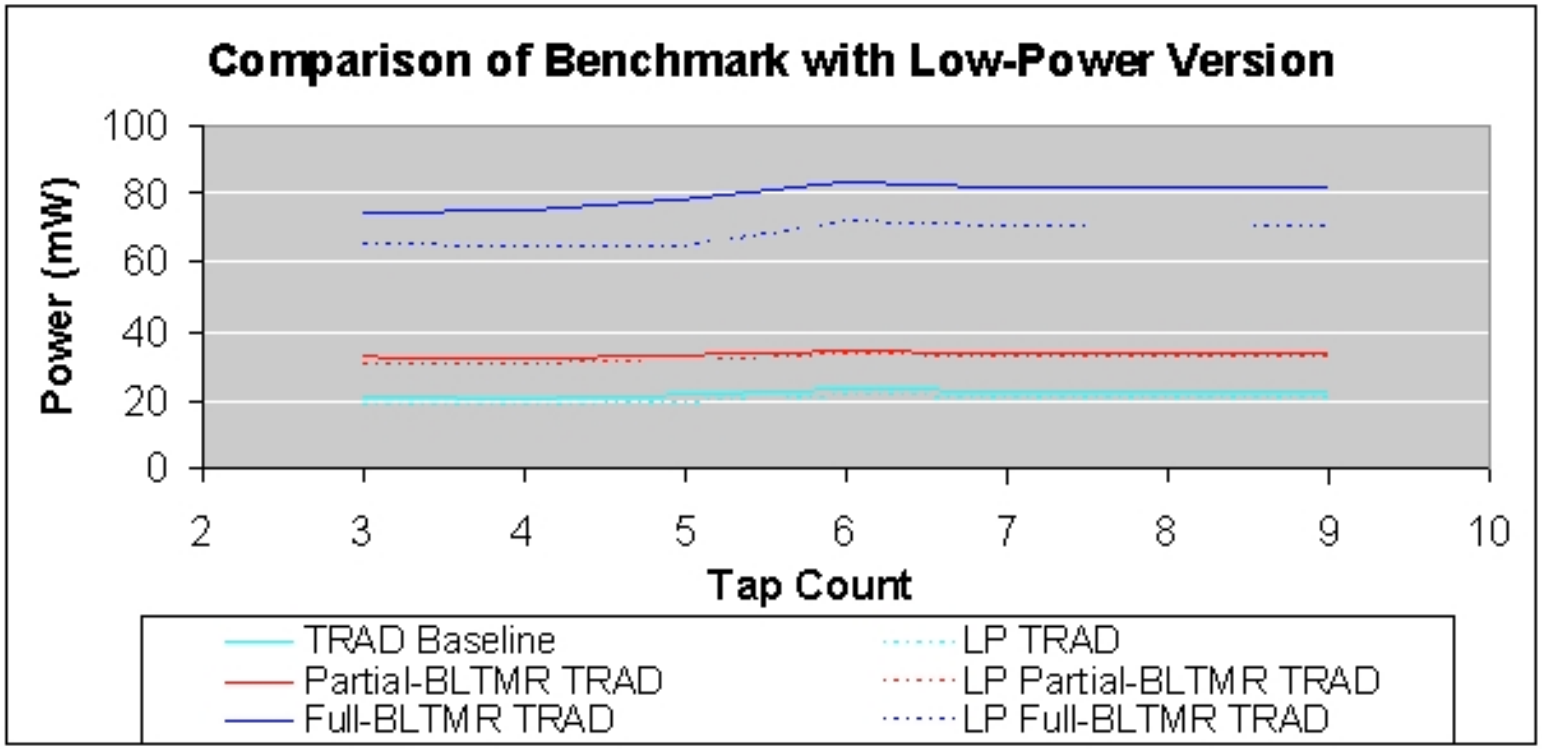
Partial BLTMR



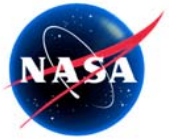
Full BLTMR



Benchmark Power Optimization



- **Baseline Power Improvement: 8.4%**
- **Partial-BLTMR Power Improvement: 4.5%**
- **Full-BLTMR Power Improvement: 14.2%**



Power Optimization Algorithm Analysis

- **Which algorithms perform best with redundancy mitigation techniques?**
- **2-terminal net co-location**
  - **TMR designs respond well**
  - **More opportunities to optimize signal power**
  - **Less adverse effects on crowded circuits.**
- **Slack minimization**
  - **Some savings for all three designs (baseline, partial, full)**
  - **Best for non-TMR circuit**
    - **Small circuits have more slack and thus have more opportunity to optimize**
- **Clock paring**
  - **Best approach**
  - **Universal power consumer**
  - **All designs yield good results**

Mitigation Validation: SEU Emulation

- **Fault injection performed in hardware to identify the number of programming bits that can cause output errors if changed (i.e., "sensitive programming bits")**
- **These bits are then processed with our SEU persistence simulator to evaluate how persistent errors are after the programming data erors have been corrected (i.e., "persistent error programming bits")**
- **Identical hardware used for radiation testing**

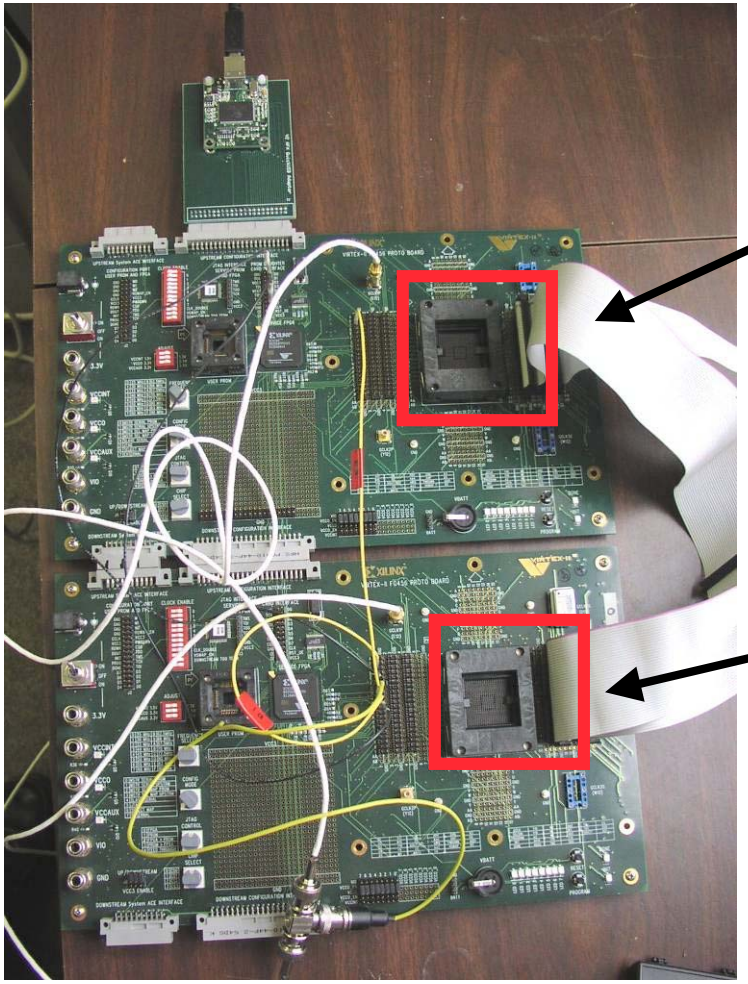


Image Convolution Designs: SEU Emulator

Design	Total Programming Bits	Sensitive Design Bits	Persistent Design Bits	% Sensitive	% Persistent	Persistent/ Sensitive
Baseline	3744736	26295	11819	0.70%	0.32%	45%
Low-power baseline	3744736	29095	17069	0.78%	0.46%	59%
Partial TMR	3744736	23263	6973	0.62%	0.19%	30%
Low-power Partial TMR	3744736	24755	7498	0.66%	0.20%	30%
Full TMR	3744736	1846	1225	0.05%	0.03%	66%
Low-power Full TMR	3744736	2041	1218	0.05%	0.03%	60%

Accelerator Results: Image Convolution Design (Adjusted for BRAM upsets)

	SEU Emulator		Accelerator (BRAM adjusted)			
Design	**Sensitivity (%)**	**Persistence (%)**	**Sensitivity % (Total Events)**	**Persistence % (Total Events)**	**Total Upsets (estimated)**	**% of bitstream upset**
Baseline	0.70%	0.32%	0.66% (81)	0.14% (17)	12214	0.33%
Low-power baseline	0.78%	0.46%	N/A	N/A	N/A	N/A
Partial TMR	0.62%	0.19%	N/A	N/A	N/A	N/A
Low-power Partial TMR	0.66%	0.20%	0.61% (50)	0.02% (2)	6291	0.22%
Full TMR	0.05%	0.03%	0.17% (24)	0.08% (12)	14470	0.39%
Low-power Full TMR	0.05%	0.03%	0.86% (181)	0.12% (25)	21075	0.56%

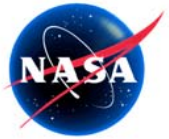


Image Convolution: SEU Emulation (Summary)

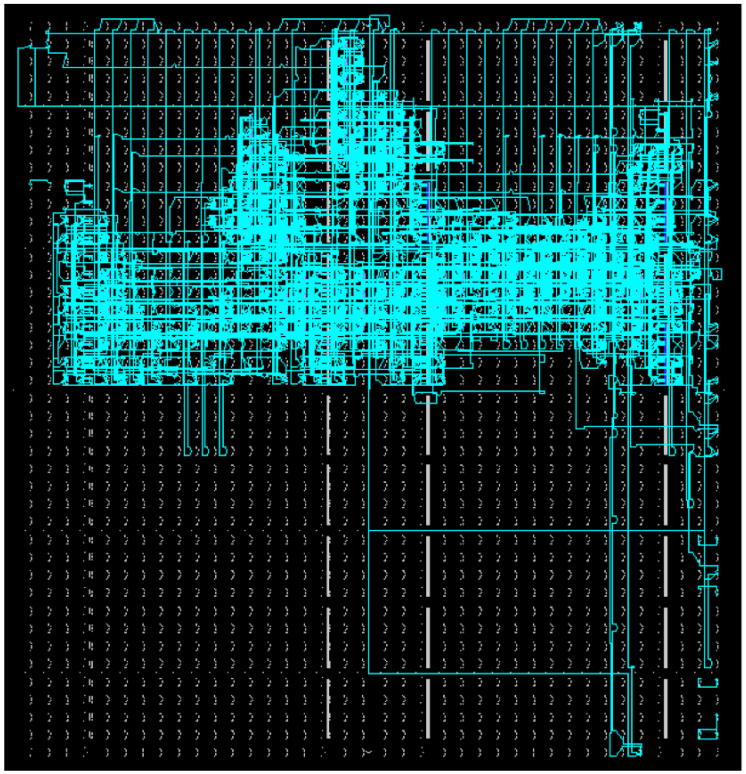
- **Impact of full TMR vs. no TMR**
  - **Sensitivity: 93% reduction**
  - **Persistence: 90-93% reduction**
  - **Area: 400% more slices (5x), 290% more LUTs (3.9x), 200% more BRAM/Multipliers/flip-flops (3x)**
  - **Not 100% since clocks and other circuit inputs/outputs not triplicated, but BLTMR working well**
- **Impact of partial TMR vs. no TMR**
  - **Partial mitigation covers only the feedback portions of the circuit (inputs and outputs of feedback section are unmitigated)**
  - **Sensitivity: 12-13% reduction**
  - **Persistence: 41-56% reduction (targeted TMR working!)**
  - **Area: ~150% more slices (2.5x), 204% more LUTs (3.04x), 52% more flip-flops (1.52x), no additional BRAM or Multipliers**

Impact of Low-power Optimizations on SEU Sensitivity

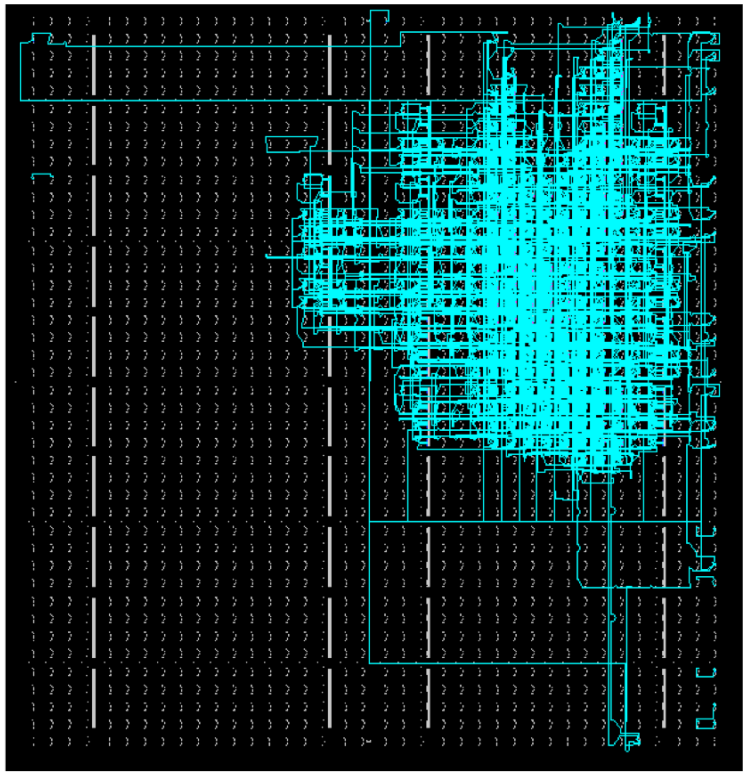
- **Low-power optimizations on EDIF netlists through timing and location constraints increased the design sensitivity**
  - **6.4 – 10.4% increase in sensitive bits compared to baseline (Relative Errors)**
- **However with 3.7 million bits, absolute increase in sensitive bits is small**
  - **Total sensitive bits increase by ~0.00 – 0.08% (Absolute Errors)**
  - **Minimal change to cross section**
- **Why?**
  - **Hypothesis: Nearly identical logic and memory resources suggests that it has to be related to routing, so the average number of programming bits used per wire is higher.**
    - **This may be true despite the decrease in clock routing since the overall number of wires in the design dwarfs the number of clock wires.**
    - **May also be a result of increased routing congestion as well as distances between resources.**

Sensitivity Increase with Low-Power Optimization

FPGA Design Layout is greatly affected by the power optimization.



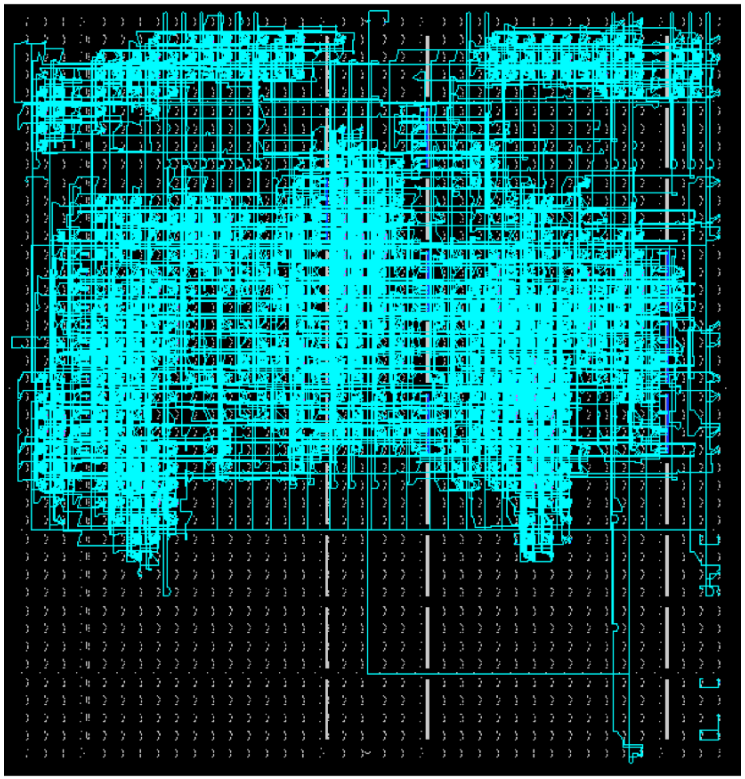
Baseline (No TMR or power opt)



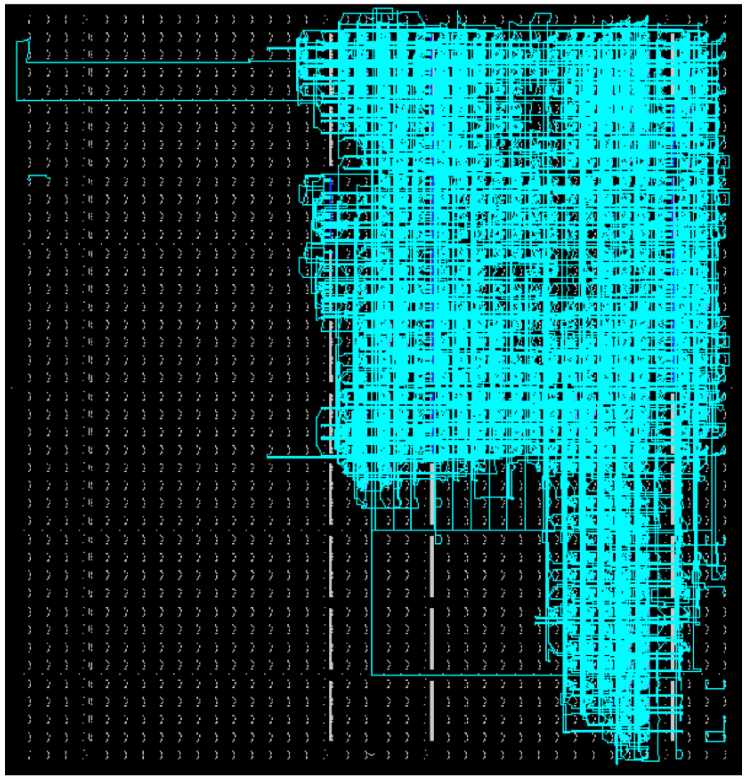
Low-power Baseline (No TMR, power opt)

Sensitivity Increase with Low-Power Optimization

FPGA Design Layout is greatly affected by the power optimization.



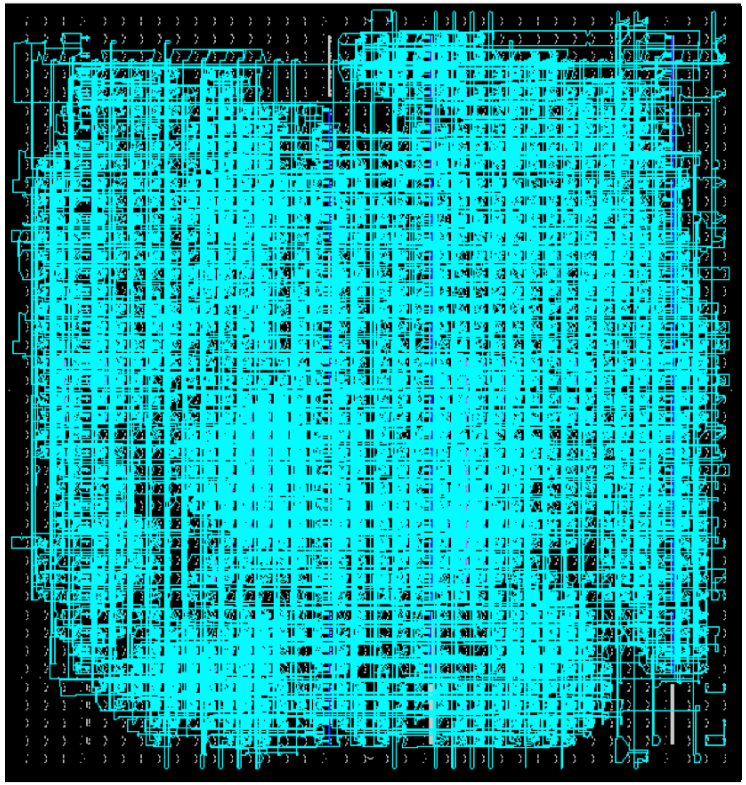
Partial TMR (partial TMR, no power opt)



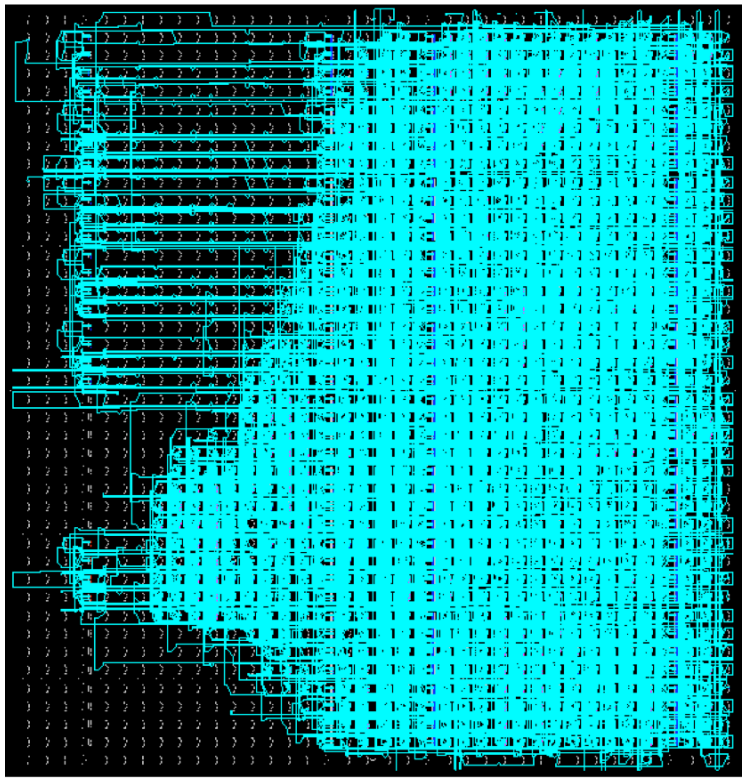
Low-power, *Partial TMR* (partial TMR, power opt)

Sensitivity Increase with Low-Power Optimization

FPGA Design Layout is greatly affected by the power optimization.



Full TMR (full TMR, no power opt)



Low-power Full TMR (full TMR, power opt)

Summary

- Partial TMR allows variable reliability and power utilization
  - Enables 25 – 50% reduction in size and power
- Power optimization techniques for ground-based circuits work well on TMR designs as well
  - Up to 14% dynamic power reduction
- Optimizing routing for power has minimal impact on reliability
  - ~0.00 – 0.08% increase in absolute sensitive cross section
- SEU emulator key for expediting and facilitating laboratory and relative environment testing
  - Identical hardware and software environment
  - Selectively corrupt every bit
- Multi-Bit Upsets (MBUs) studied
  - Not yet a problem at 130nm, concern at 90nm and beyond
- http://rhino.east.isi.edu
  - Code open source and downloadable
  - 15 conference and journal papers

COTS FPGA devices can be meet space environment demands with common CAD tool

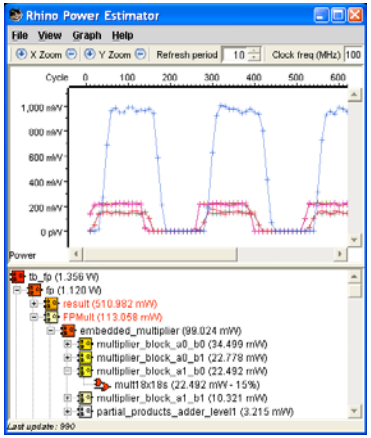
Reconfigurable Hardware in Orbit (RHinO)

PI: Matthew French, USC / ISI

Objective

- Facilitate and Automate Designing an SRAM-based FPGA Circuit for the Space Environment
- Create a CAD tool Environment for Xilinx Virtex-II SRAM-based FPGAs capable of
  - **Mitigating Transient Effects**
  - **Minimizing Power Utilization**
- Provide an Extensible Infrastructure for Future Tests, Techniques, and Architectures

SEU Emulator



Power Tools

Accomplishments

- Developed end-to-end tools for Virtex2 radiation mitigation and power optimization that interoperate with the COTS tool flow
- Radiation Mitigation: Developed partial TMR technique which results in 25 to 50% reduction in size and power
- Power Optimization: Developed power optimization techniques that yield 5 to 15% dynamic power reduction on partially TMR circuits
- An SEU Hardware Emulator for Virtex2 was developed, which predicts radiation results and reduces the amount of necessary radiation testing

CoAI: Tools and emulators verified in experiments at U.C. Davis and Lawrence Berkeley radiation facilities

Paul Graham, Los Alamos National Laboratory
Michael Wirthlin, Brigham Young University

TRL_{in} = 3; TRL_{out} = 6